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**REMARKS**

Claims 1-3 and 7-23 are all the claims presently pending in the application. Claims 4-6 were previously canceled. Claims 1, 7, 9, 10, 17, 20 and 22-23 were amended. Claims 1, 17, 18, 20, and 21 stand rejected under 35 U.S.C. § 112, first paragraph. Claims 1-3 and 7-23 stand rejected on prior art grounds.

Claims 1-3 and 7-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamane, et al. (U.S. Pat. No. 6,020,229) in view of Mori, et al. (U.S. Pat. No. 6,376,879 B2).

These rejections are respectfully traversed in view of the following discussion.

Entry of this 1.116 Amendment is proper. Since the amendments above narrow the issues for appeal and since such features were in the claims earlier, such amendments do not raise a new issue requiring further searching and/or consideration by the Examiner. As such entry of this Amendment is believed to be proper and is earnestly solicited.

It is noted that the amendments are made only to more particularly define the invention and not for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

**I. THE CLAIMED INVENTION**

Applicant's invention, as disclosed and claimed, for example by claim 1, and similar independent claims 22 and 23, is directed to a semiconductor device.

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The semiconductor device includes a plurality of transistors comprising different gate insulator film in their thickness value, the plurality of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof. The plurality of transistors include lightly doped drain regions. The gate electrode includes an impurity to suppress depletion which is implanted when forming the lightly doped drain regions, and the lightly doped drain region have depths corresponding to the thickness values of the gate electrode and the gate insulator film. (See Page 5, lines 1-10; Page 11, lines 1-11 and 18-24; Page 12, lines 1-10 and 20-24; Page 15, line 20-Page 16, line 11; and Figures 3(I)-(L)).

Conventional NMOSFET devices include the same gate electrode as a mask for both the core-purpose MOSFET and the I/O-purpose MOSFET. However, these devices restrict energy (ion) implantation into the lightly doped drain region making it very problematic to dope an impurity to a deep level thus forming shallow lightly doped drain regions with strong electric fields at the drains, which increase breakdown effects and give rise to hot carriers deteriorating the reliability of the device. (See Page 3, lines 3-8; Page 8, line 20-Page 9, line 5; Page 12, lines 1-10).

In inventive device, on the other hand, the plurality of transistors include lightly doped drain region have depths corresponding to the thickness values of the gate electrode and the gate insulator film. This feature reduces the electric field in the space region and efficiently suppresses the occurrence of a hot carrier and optimizes high-voltage reliability. (See Page 5, lines 1-10; Page 11, lines 8-11; Page 12, lines 1-10 and 20-24; Page 13, lines 1-7; Page 15, line 20-Page 16, line 11; and Figures 3(I)-(L)).

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As a result, the claimed invention provides a semiconductor device with an increased process margin of the gate etching during manufacturing and improved performance. (See Page 5, lines 7-10; Page 12, lines 11-25).

## II. THE 35 U.S.C. § 112, FIRST PARAGRAPH REJECTIONS

Applicant has amended claim 1 in response to the 35 U.S.C. § 112 rejection by clarifying that, "the gate electrode includes an impurity to suppress depletion which is implanted when forming the lightly doped drain regions, and the lightly doped drain regions have depths corresponding to the thickness values of the gate electrode and the gate insulator film." (See Specification, Page 12, lines 1-10 and 20-24; and Page 15, lines 19-24).

Further, Applicant has amended claims 17 and 20 to clarify that the lightly doped drain region comprises a well with an N - type impurity "implanted at a predetermined density and a predetermined energy level used for implantation." Since these changes are consistent with the Specification at Page 12, lines 1-10, Applicant traverses the assertion that new matter has been added. The Amendments to claims 17 and 20, accordingly, should obviate the need to amend claims 18 and 21.

In view of the foregoing, the Examiner is respectfully requested to withdraw these rejections.

## III. THE PRIOR ART REJECTIONS

### A. The 103(a) Rejection Based on Yamane, et al. in view of Mori, et al.

First, the references, separately, or in combination, fail to teach, disclose or provide a reason or motivation for being combined. In particular, Yamane, et al. ("Yamane") pertains

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to a semiconductor device, and related method, including a thin film polysilicon film used as a resistive element having a small parasitic capacitance, with a non-volatile memory operating at high speed and high reliability. (See Yamane at Abstract; Column 1, lines 5-30; and Column 2, line 65 - Column 3, line 15).

By contrast, Mori, et al. ("Mori") does not have the same aim as Yamane.

Mori discloses a semiconductor device having MISFETs with at least two operating voltages, such as a flash EEPROM, and a self-alignment structure "serving to increase the integration density of an LSI ("Large Scale Integration") without causing an increase in the contact resistance." (See Mori at Abstract; Column 1, lines 5-15; and Column 5, lines 20-30).

Nothing within Yamane, which relates to a non-volatile memory operating at high speed and high reliability with gate electrodes of different thicknesses, suggests a MISFET with at least two operating voltages and a self-alignment structure to increase the integration density of an LSI with gate electrodes of the same thickness as disclosed in Mori. Thus, Yamane teaches away from being combined with another invention for example Mori.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight. It is clear that the Examiner has simply read Applicant's specification and conducted a keyword search to yield Yamane and Mori. Further, the Examiner provides no motivation or reason to combine, other than to assert that it would have been obvious to one having ordinary skill in the art, "to combine, the teaching of Mori and Yamane in order to have Ldd regions since a Ldd structure performs functions of increasing the breakdown voltage, migrating of the hot carriers and inhibiting short channel effects" and "to form [a] deeper drain region including LDD regions as suggested by Mori to withstand higher operating voltage." Such an assertion does not take into account the distinct structural

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differences of the two inventions as indicated above, and further discussed below. Thus, the Examiner's assertion attempts to solve a potential problem which does not ever exist with either Yamane or Mori, and this assertion is further proof of the Examiner's use of impermissible hindsight.

Secondly, even if combined, the references do not teach or suggest at least one of the two features of independent claim 1, and similar claims 22 and 23, including the lightly doped drain region have depths corresponding to the thickness values of the gate electrode and the gate insulator film.

The Examiner admits Yamane, as indicated above, does not teach or suggest features of independent claim 1, and similar claims 22 and 23, including "Ldd [lightly doped drain] formation," let alone, the plurality of transistors include lightly doped drain regions. (See Office Action at Page 3, 3<sup>rd</sup> Paragraph). Yamane does not teach or suggest including that the lightly doped drain region have depths corresponding to the thickness values of the gate electrode and the gate insulator film.

Mori fails to make up for the deficiencies of Yamane.

Instead, in Figures 8 and 9 of Mori, Mori discloses a semiconductor device having MISFETs with at least two operating voltages, such as a flash EEPROM, and a self-alignment structure. (See Mori at Abstract; Column 1, lines 5-15; and Column 5, lines 20-30). This structure includes lightly doped drain regions of different depths corresponding to gate electrodes having substantially identical thickness values. Please note that the thickness values are in the vertical direction.

Applicant's invention, on the other hand, includes the lightly doped drain region have depths corresponding to the thickness values of the gate electrode and the gate insulator film.

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Further, in Figure 10 of Mori, Mori shows that the high voltage gate is longer than the gate of the normal transistor. (See Figure 10). The longer gate is not necessary in the claimed invention. Also the channel region under the gate in the high voltage transistor likely has impurities because the gate is no thicker than the normal transistor. (See Application, Page 3, lines 3-8).

Indeed, unlike the claimed invention, Mori is focused on providing a structure in which "each low voltage transistor helps to enhance the integration density of the semiconductor device (LSI) because it has a self-alignment contact structure and a short LDD length[.]" and "[t]he breakdown voltage of the p-n junction can, therefore, be increased in the high voltage transistor" (See Mori at Abstract; Column 1, lines 5-15; Column 5, lines 20-30; and Column 10, lines 53-65). Mori, however, does not teach, disclose or suggest, the lightly doped drain region have depths corresponding to the thickness values of the gate electrode and the gate insulator film. Consequently, Mori does not teach, suggest or disclose Applicant's invention.

Accordingly, Applicant traverses the assertion in the Office action that Mori teaches "a device with Ldd formation in HV transistor and Normal transistor which have different sizes in a gate insulator film and a gate electrode" as teaching or suggesting Applicant's invention. (See Office Action at Page 3, 3<sup>rd</sup> Paragraph; and Page 5, 4<sup>th</sup> Paragraph-Page 6, 1<sup>st</sup> Paragraph).

For at least the reasons outlined above, Applicant respectfully submits that neither Yamane nor Mori teach or suggest all of the features of independent claims 1, 22 and 23, and related dependent claims 2-3 and 7-21. These dependent claims are patentable not only by virtue of their dependency from their respective independent claims, but also by the additional limitations they recite.

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For the reasons stated above, the claimed invention, and the invention as cited in independent claims 1, 22 and 23, should be fully patentable over the cited references.

#### **IV. FORMAL MATTERS AND CONCLUSION**

In view of the foregoing, Applicant submits that claims 1-3 and 7-23, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

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The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 6/13/03

  
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**CERTIFICATION OF FACSIMILE TRANSMISSION**

I hereby certify that I am filing this Amendment by facsimile with the United States Patent and Trademark Office to Examiner Junghwa M. Im, Group Art Unit 2811 at fax number (703) 872-9319 this 13th day of June, 2003.

  
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